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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,051	03/12/2001	Salman Akram	MIO 0069 PA	7513

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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/804,051	AKRAM ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9 and 25-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9 and 25-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *063003* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 8 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Akram (US 6,300,163).

3. Claims 1 and 8 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hsuan (US 6,236,109).

4. Claims 1, 8, 25-29 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Yenkateshwaran (US 6,388,336).

5. Claims 1 and 29-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Moden (US 6,303,981).

6. Moden (Fig 2A,D) discloses a multiple die semiconductor assembly comprising a first semiconductor die (16A) defining a first active surface (bottom portion), including at least one conductive bond pad (34A); a second semiconductor die (16B) defining a second active surface (top portion) including at least one conductive bond pad (34B); and a single intermediate substrate (24A,B) positioned between said first semiconductor die and said second semiconductor die such that a first surface (top portion) of said

intermediate substrate faces said first semiconductor and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein said intermediate substrate defines a passage there through, and one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces; wherein said first die comprises a stacked chip secured to said first surface of said intermediate substrate such that said conductive bond pads on said first active surface are align with said passage (via space between leads); further comprises conductive lines (36A) extending from said conductive bond pads on said first active surface to conductive contacts on said second surface of said intermediate substrate; said conductive bond pad on said second active surface is aligned with said passage; and conductive lines extending from said conductive bond pads on said second active to conductive contacts on said first surface of said intermediate substrate; wherein said first and second die is electrically coupled to said intermediate substrate (via line, 36A,B); and said first is electrically coupled to said second die (via 18A contact 18b; Fig 2A); with said second semiconductor die electrically coupled to said intermediate substrate by at least one conductive line (36B) extending from said conductive bond pad (34B) of said second semiconductor die through said passage defined in said intermediate substrate and to said first surface of said intermediate substrate; wherein said assembly further comprises an underfill material/ encapsulant (12; top portion; Fig 2D, and A) formed over said first surface of said intermediate substrate and said first die; and between said first die and said first surface of said intermediate substrate; with an encapsulant formed

over said second semiconductor die; and a die attach adhesive (20A,B) positioned to secure said second semiconductor die to said second surface of said intermediate substrate.

7. Claims 4, 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Yenkateshwaran et al. (US 6,388,336).

8. Yenkateshwaran (Fig 2) a multiple die semiconductor assembly comprising: a first semiconductor die (25a) defining a first active surface (25b) including at least one conductive bond pad (not shown); a second semiconductor die (21a) comprising a second active surface (21b), said second active surface including at least one conductive bond pad (21c); an intermediate substrate positioned between said first active surface of said first die and said active surface of said second die, such that a first surface (via top surface) of said intermediate substrate faces said first semiconductor die and such that a second surface (via bottom) of said intermediate substrate faces said second semiconductor active surface, wherein said first die is electrically coupled to said intermediate substrate by at least one topographic contact (26) extending from said first active surface to said first surface of said intermediate substrate, said intermediate substrate defines a passage there through, said second semiconductor die is secured to said second surface of said intermediate substrate such that said conductive bond pad of said second semiconductor die is aligned with said passage, and said second semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line (24) extending from said conductive bond pad of said second semiconductor die through said passage defined in

said intermediate substrate and to a conductive contact (via surface) on said first surface of said intermediate substrate; said topographic defines a space between said first surface and said first surface of said intermediate substrate.

9. Claim 5 rejected under 35 U.S.C. 102(e) as being anticipated by Hur (US. 6,646,334).

10. Hur discloses a multiple die semiconductor assembly comprising: a first semiconductor die (top) defining a first active surface, said first active surface including at least one inherent conductive bond pad (via surface contact with wire), a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad; an intermediate substrate positioned between said second semiconductor die and said first active surface of said first semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second semiconductor die wherein said intermediate substrate defines a passage there through, said first semiconductor die is secured to said first surface of said Intermediate substrate such that said conductive bond pad of said first semiconductor die is aligned with said passage, and said first semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line (wire; not labeled) extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said second surface (bottom) of said intermediate substrate; and an additional substrate (via middle leads; not labeled) positioned such a first surface (top) of said additional

substrate faces said second active surface of said second semiconductor die and such that said first surface of said additional substrate opposes (facing each other) said second surface of said intermediate substrata wherein said additional substrate defines an additional passage therethrough, said second semiconductor die (middle) is secured to said first surface of said additional substrate such that said conductive bond pad (not labeled) of said second semiconductor die is aligned with said additional passage, said second semiconductor die is electrically coupled to said additional substrate by at least one conductive line extending (middle wire) extending from said conducive bond pad (not labeled) of said second semiconductor die through said additional passage defined in said additional substrate and to a conductive contact on a second surface (bottom) of said additional substrate.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2, 6, 9 and 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yenkateshwaran (US 6,388,336) and further in combination with Suzuki et al (US 5,532,910).

13. Yenkateshwaran discloses the elements stated in paragraph 8 of this office action, but does not appear to disclose at least one decoupling capacitor decoupling capacitor conductively coupled to at least one of said first and

second semiconductor dies. wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die.

14. However Suzuki utilizes a decoupling capacitor accommodated in a space.

15. It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor in contact with a leadframe of Yenkateshwaran, such that it would be accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die, in order to remove noise as taught by Suzuki (Col. 1, Lines 48).

16. Claim 7, 49 and 50-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hur (US 6,646,334) in combination with Suzuki et al (US 5,532,910).

17. Hur discloses the elements stated in paragraph 10 of this office action and further shows a third substrate (bottom lead) positioned such that a first surface (top portion) of said third substrate faces said second surface of said additional substrate, with said additional substrate is electrically coupled (via vertical conductive portions; not labeled) to said third substrate by at least one topographic contact extending from said second surface of said additional substrate to a first surface (top) of the said third surface, and

with the second surface of said third substrate faces a first surface of said intermediate substrate (via substrate surfaces are considered either 1st or 2nd surface).

18. Hur does not appear to disclose at least one decoupling capacitor decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies. wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die.

19. However Suzuki utilizes a decoupling capacitor accommodated in a space.

20. It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor in contact with a leadframe of Hur, such that it would be accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die, in order to remove noise as taught by Suzuki (Col. 1, Lines 48).

21. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Hsuan (US 6,236,109) as applied to claim 8 and further in combination with Suzuki et al (US 5,532,910).

22. Hsuan does not appear to disclose at least one decoupling capacitor decoupling capacitor conductively coupled to at least one of said first and second semiconductor

dies. wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die.

23. However Suzuki utilizes a decoupling capacitor accommodated in a space.

24. It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor in contact with a leadframe of Hsaun, such that it would be accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, a topographic contact conductively coupled to said first semiconductor die, and a topographic contact conductively coupled to said second semiconductor die, in order to remove noise as taught by Suzuki (Col. 1, Lines 48).

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 6:30-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jmm

DAVID E. GRAYBILL
PRIMARY EXAMINER